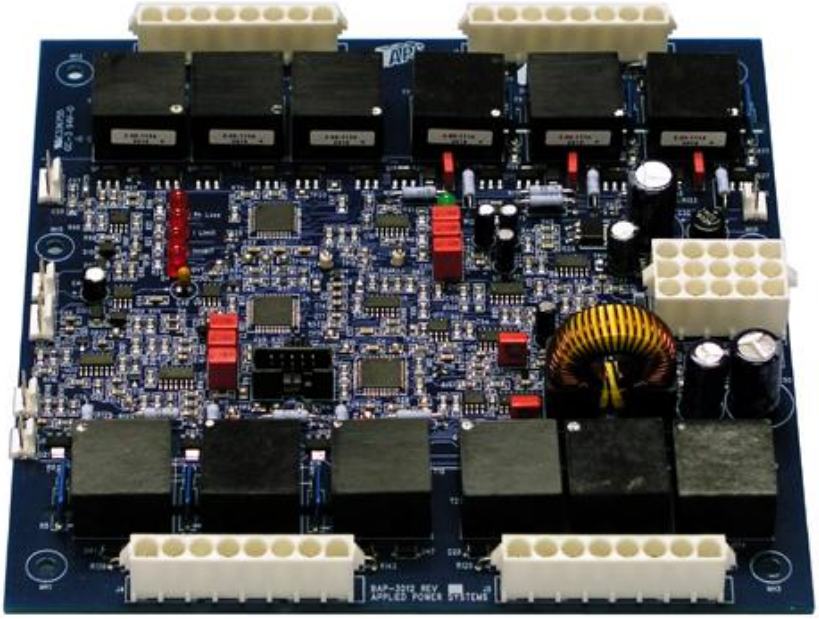
APPLIED POWER SYSTEMS, INC.

BAP3012 Twelve-Pulse SCR Control Board

TWELVE PULSE SCR CONTROL BOARD

- **Matches paralleled bridge currents to within 1%**
- **Complete control of 12-Pulse Converters and Controllers**
- **Reduces output voltage ripple and input harmonics**
- **On board Current Limit potentiometer**
- **Overtemperature protection of semiconductor devices**



Advancing the State-of-the-Art in SCR Gate Firing

The BAP3012 is the latest generation twelve pulse control board for SCR control. Standard BAP3012 features provide robust and reliable operation driving parallel or series connected bridges.

BAP3012 standard features include:

- instant inhibit
- phase loss inhibit
- soft start & soft stop functions
- controls AC main voltages up to 600 VAC
- on-board diagnostic LED indicators
- on-board current limit control
- active balancing of current in parallel bridges within 1%

The BAP3012 provides complete SCR firing control for industrial/commercial power supplies of any power level, delivering hard firing gate drive power to control larger SCRs from 16mm to 100mm.

The BAP3012 allows the user to take advantage of the benefits inherent to 12 pulse converters. These topologies provide very low output voltage ripple and minimize input harmonic distortion. In order to fully take advantage of phase shifted bridge topologies, the current output of each bridge must be balanced. Slight mismatches, of as little as 0.5% in transformer secondary voltages can result in current imbalances between paralleled bridges as high as 20%.

The BAP3012 directly interfaces with low cost Hall Effect sensors or an optional shunt interface circuit to monitor and actively force the currents out of each bridge to be matched within 1%. With a minimal inductance inserted in series with each bridge, the BAP3012 will independently adjust the delay angle of each bridge to actively force the currents to be the same.

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Functional Description

Signal Conditioning of Input Return

Controlling SCRs requires varying the conduction angle to control the portion of the input voltage that is conducted to the output. The BAP3012 has two phase locking circuits that independently phase lock to both transformer secondaries, which creates the phase references required to control the conduction angle of the six SCRs in each bridge. Phase references are derived for each bridge from the cathodes of the three lower SCRs on J2 and J4 (refer to Figure 2). The signals used to create the phase references are filtered in order to remove unwanted harmonics that will affect the precision with which the delay angles are controlled for each bridge.

The phase rotation of both three-phase inputs is sensed and the SCR gating is automatically adjusted to account for either ABC or ACB rotation. Therefore, either three-phase input source cannot be connected with an incorrect phase rotation.

SCR Gating Phase Locked to the Utility Input

In order for the delay angle to control the conduction angle of the SCRs, the delay angle must be phase locked and then phase shifted from the utility input by an amount determined by the delay angle control. The BAP3012 uses an independent phase locked loop circuit for each bridge to keep the SCR gating signals in phase with its respective three-phase input.

Delay Angle Control

The magnitude of the delay angle control input determines the point on the input waveforms that all SCRs will be switched on, which will control the output voltage of a Converter (AC in, DC out) or an AC Controller (AC in, phase-controlled AC out). The BAP3012 will accept a single control voltage from the user from which it derives two separate delay angle control voltages, one for each bridge. This allows the board to independently adjust each delay angle control voltage based on feedback current to actively force the output current from each bridge to be matched to within 1%.

The default scaling for the Delay Angle Control input is:

- 0V corresponds to maximum delay angle (minimum output voltage)

And

- 5V corresponds to minimum delay angle (maximum output voltage)

The scaling of the input control voltage can be modified to accept other control voltages, consult factory.

In order to provide a controlled and orderly start up sequence, the delay angle commanded by the user is not instantly applied to the SCRs at turn-on. At start up, the delay angle is forced to the maximum value. When the SCR control signals are phase locked to the input references, with no errors present, the delay angle will ramp down from the maximum value to the programmed value in approximately 400mS (this time is under microprocessor control and may be modified at the factory upon customer request). While in operation, the SCR gate firing can be turned off using either the soft stop function (shorting J6-12 to J6-11) or the fast turn off feature (open the contact closure between J6-4 and J6-6). When the soft stop is used, the delay angle will ramp up to its maximum value in approximately 100mS (this time may also be modified at the factory upon customer request). If the board is forced into a fast turn off condition, all SCR gate signals will be logically inhibited within 1mS.

Logic Implementation

Each bridge will have a dedicated FPGA (Field Programmable Gate Array) that will perform all of the logic required to control the delay angle. Since they are programmable, they can be modified to adapt to customer needs in certain applications, at the factory, when ordered.

DC Gate Drive

The BAP3012 comes equipped with DC gate drives, rather than picket fence drives, which offers improved performance in circuits with discontinuous load currents. If an SCR loses its holding current when being driven with a picket fence, the SCR can turn off and may not turn on again until the next series of gate pulses. The DC drive keeps current flowing into the gate so that the SCR will continue to be commanded on for the entire time that the SCR is in conduction.

The current waveform sourced to each SCR gate has an initial 2.4 Amp peak pulse approximately 20µS wide, followed by 800 mA of DC current for the remainder of the turn-on signal. The open circuit voltage applied to the gate is 24 volts, which enables the BAP3012 to drive large area devices under high *di/dt* conditions.

Options for Powering the Board

The BAP3012 may be powered from a 24 VAC source connected across J6-1 and J6-2, OR powered from a 30 VDC source connected to J6-3 returned to J6-8. While running from either an AC or DC source, the board will consume a maximum of 15 VA.

Fault Detection and Shut Down Sequence

If one or all of the input phases are lost, the PHASE LOSS LED is illuminated and a fast turn off is initiated which inhibits all gate signals within 1mS. When the lost phase is restored, the unit will ramp up to the programmed delay angle in 400mS.

A fast turn off can also be initiated by removing the contact closure between J6-4 and J6-6. This type of turn off digitally inhibits all gate signals. If a soft turn off is desired, a contact closure should be connected across J6-12 and J6-11. This will ramp the delay angle to a maximum value (resulting in minimum output voltage) in 100 mS. At this point, the board is sourcing gate drive signals that are at a maximum delay angle, resulting in 0 volts in first quadrant operation. Either of these conditions will illuminate the INHIBIT LED.

If the optional temperature sensing circuit is used, the OVERTEMP LED will be illuminated and the gate signals are inhibited 1mS after the over temperature threshold is exceeded. The default value for the over temperature threshold is 90ºC. The delay angle will ramp down to the programmed value after the heatsink temperature drops to 85°C. This value of thermal hysteresis can be modified to suit the customer's requirements.

Current Balancing Scheme

What sets the BAP3012 apart from other 12 pulse controllers is its ability to force the currents out of 2 paralleled six pulse bridges to be matched to within 1%. Current feedback from either Hall Effect sensors or shunts monitoring the current out of each bridge is used to independently adjust the delay angle control voltage for each bridge to match the currents.

The reason for the diverging currents is often due to the input transformer. System designers are at the mercy of transformer manufacturers that attempt to match the turns ratios of both delta and wye secondaries. The deviation in primary to delta and primary to wye ratios often results in two paralleled secondary bridges with slightly different output voltages, which may result in significantly different bridge currents. The BAP3012 will constantly read the current out of each bridge and actively correct any imbalances.

The BAP3012 interfaces directly with the HAS, HAC, or HAX series Hall Effect sensors from LEM or equivalent. The current magnitude out of each bridge will determine the current rating of the transducer or shunt. If a shunt is the current sensing device of choice, then an additional circuit board to interface with the BAP3012 can be purchased from APS. Please contact APS for further information.

Current Limit

A potentiometer allows the user to vary a current limit threshold that, when reached, will prevent any additional current from being sourced by the SCR bridges. The pot may be on board or remotely mounted depending on customer requirements. Series connected bridges require only one current sensor.

Connectors

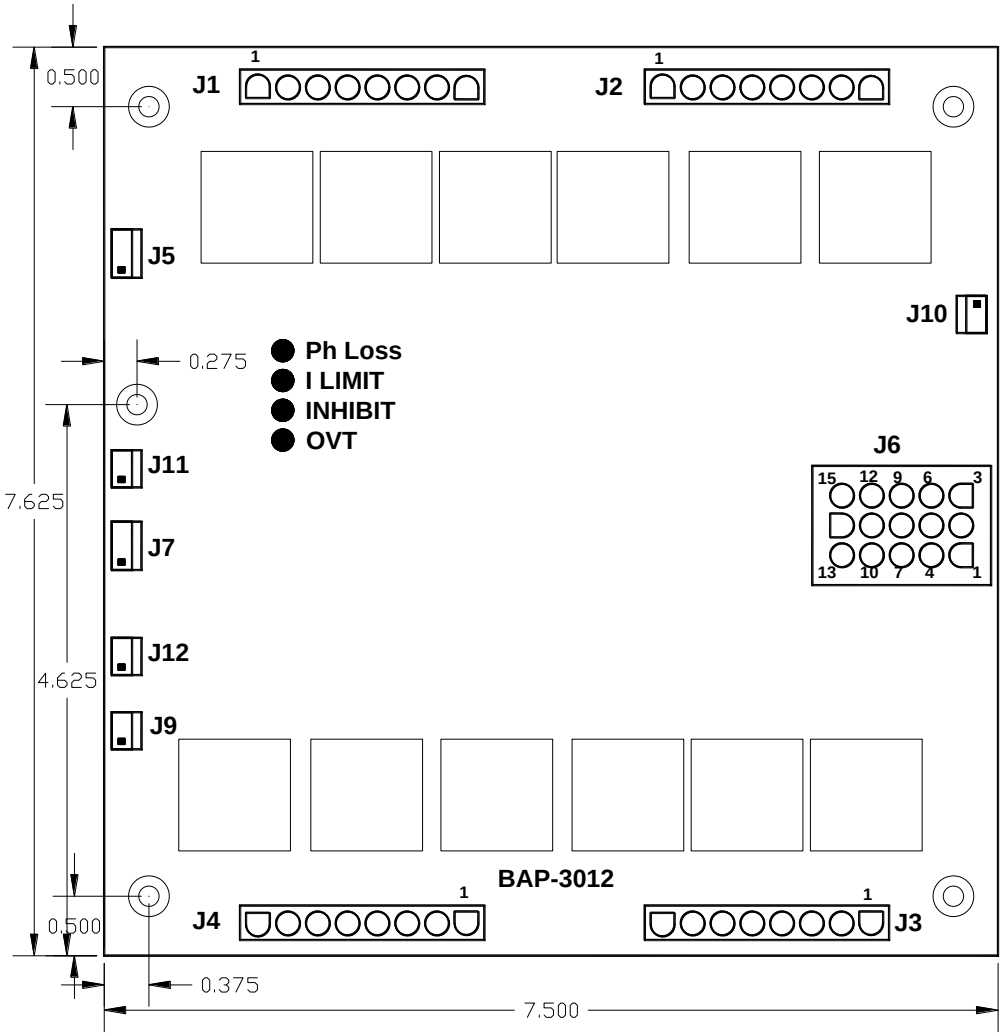

Figure 1: Connector Layout

Gate Drive Connectors J1, J2, J3, and J4

Four Mate-N-Lok™ type connectors allow for a convenient interface with the SCR gates. The mates for these connectors are supplied with the board along with keying plugs to eliminate the possibility of inadvertently swapping J1 and J2 or J3 and J4.

Each connector has three pairs of wires to drive three SCRs. J1 and J3 are configured to drive the three upper SCRs in a converter topology.

J2 and J4 are configured to drive the three lower SCRs in a converter topology or the three SCRs with the cathodes connected to the utility in an AC controller. The phase reference signals for both phase locked loops are obtained from the J2 and J4 connectors. The cathode connections of the gate drives to the lower SCRs serve as the phase reference signal inputs. Refer to Figure 2. However, if the BAP3012 is controlling an ANSI 45-46 topologies (sometimes referred to as a Star configuration), the phase reference signals can be obtained via connectors J9 and J10. Note that J9 and J10 are scaled for voltages less than 50 Vrms. If larger voltages are controlled with this topology, an interface board may be obtained from APS.

Please refer to Figure 2 for the following connections

J1 Connector – Gate Drive Connector

Pin	Signal Name	Description
1	Blank	
2	Keying Plug	
3	A1+ Gate	Gate drive for phase A1; upper SCR in converter
4	A1+ Cathode	Gate return for A1+
5	B1+ Gate	Gate drive for phase B1; upper SCR in converter
6	B1+ Cathode	Gate return for B1+
7	C1+ Gate	Gate drive for phase C1; upper SCR in converter
8	C1+ Cathode	Gate return for C1+

J2 Connector – Gate Drive Connector and phase reference inputs

Pin	Signal Name	Description
1	A1- Gate	Gate drive for phase A1; lower SCR in converter
2	A1- Cathode	Gate return for A1-; used to derive phase A reference
3	Keying Plug	
4	B1- Gate	Gate drive for phase B1-; lower SCR in converter
5	B-1 Cathode	Gate return for B1-; used to derive phase B reference
6	Blank	
7	C1- Gate	Gate drive for phase C1-; lower SCR in converter
8	C1- Cathode	Gate return for C1-; used to derive phase C reference

J3 Connector – Gate Drive Connector

Pin	Signal Name	Description
1	A2+ Gate	Gate drive for phase A2+; upper SCR in converter
2	A2+ Cathode	Gate return for A2+
3	B2+ Gate	Gate drive for phase B2+; upper SCR in converter
4	B2+ Cathode	Gate return for B2+
5	C2+ Gate	Gate drive for phase C2+; upper SCR in converter
6	C2+ Cathode	Gate return for C2+
7	Keying Plug	
8	Blank	

J4 Connector – Gate Drive Connector and phase reference inputs

Pin	Signal Name	Description
1	A2- Gate	Gate drive for phase A2; lower SCR in converter
2	A2- Cathode	Gate return for A2-; used to derive phase A reference
3	Blank	
4	B2- Gate	Gate drive for phase B2-; lower SCR in converter
5	B2- Cathode	Gate return for B2-; used to derive phase B reference
6	Keying Plug	
7	C2- Gate	Gate drive for phase C2-; lower SCR in converter
8	C2- Cathode	Gate return for C2-; used to derive phase C reference

Control Signal Connector J6

The control signal connector, J6, is the user's interface to the BAP3012. The table below describes the pin functions of J6

The delay angle is proportional to the voltage applied to J6-10 returned to J6-11. The factory default scaling for this input is 5 volts at J6-10 will result in a minimum delay angle (maximum voltage) and 0 volts will correspond to a maximum delay angle (minimum voltage).

To enable the board, J6-4 must be pulled up to at least 5 volts. This can be accomplished by jumpering J6-4 to J6-6 (or J6-7) or the user can make this connection via a relay contact to instantly inhibit the SCR firing by opening up the contact.

The Soft Start/Soft Stop function is controlled by J6-12. A connection between J6-12 and J6-8 (or J6-11) will result in a soft stop condition, which is the delay angle ramping up to maximum value in 100 mS. When this connection is opened, a soft start cycle will begin, which is the delay angle ramping down from a maximum to the programmed delay angle at a rate that will take 400mS if the delay angle is programmed to the minimum (maximum conduction) value.

The BAP3012 annunciates to the user anytime the SCR firing pulses are inhibited by allowing J6-9 to be pulled up to a voltage determined by the user (maximum of 24 volts). Under normal running conditions, J6-9 is terminated through a 100Ω resistor connected to the drain of an enhanced FET. If the SCR gating is inhibited, the inhibit annunciate pin, J6-9, is no longer terminated (the FET is turned off) and can be pulled high via a customer provided pull up resistor.

A phase loss annunciate signal is available on J6-5. An open drain FET is pulled up to 15 volts through a 10K resistor when all phases are present. When one or more phases are missing possibly due to a blown fuse, the FET will turn on pulling J6-5 low.

If the customer chooses to power the BAP3012 with AC voltage (24 VAC), it is connected across J6-1 and J6-2. If the customer chooses to power with DC (30 VDC), the positive is connected to J6-3 and the return to J6-8 (or J6-11). The BAP3012 will consume a maximum of 15 VA while driving SCRs and less than 5 VA when the drive signals are inhibited. Two power supplies derived on the board are available for the customer, 15 volts on J6-6 and 5 volts on J6-7. The customer may draw up to 10 mA from either of these pins. Also, if the customer powers the board with the 24 VAC option, the 30 VDC (which is derived from the rectified 24 VAC) is available for the customer on pin J6-3. Drawing more than 25 mA from J6-3 or more than 10 mA from J6-6 or J6-7 may result in damage to the BAP3012.

An analog representation of the current out of the converter bridge is available on J6-15 referenced to J6-14. This value will be the summation of the bridge currents when connected in parallel or the current through both bridges when they are connected in series. This signal will be a maximum of 5 volts with the scaling adjusted to the customer's requirement.

J6 Connector – Control Signal Connector

Pin	Signal Name	Description
1	24 VAC	Supplied by customer to power board. 15 VA is required when board is driving SCRs.
2	24 VAC	Supplied by customer to power board. 15 VA is required when board is driving SCRs.
3	24 VDC (30 VDC MAX)	Supplied by customer to power board. 15 VA is required when board is driving SCRs. Twenty five mA available to customer when 24 VAC input is provided.
4	Fast Turn off	Shorting pin 4 to pin 6 or 7 enables the board. Opening pins 4 and 6 (or 7) will disable gating signals within 1mS
5	Phase Loss Annunciate	This pin is an open drain output that will go low in a phase loss condition and will be pulled up to 15 volts through a 10K resistor when all phases are present.
6	15 VDC	10mA available for customer use.
7	5 VDC	10mA available for customer use.
8	GND	Return for BAP3012 control circuitry including delay angle control, therefore it must be tied to the return of the customer provided delay angle control voltage
9	Inhibit Annunciate	Normally low through a 100Ω resistor. Transitions high through customer provided pull up in a Fast turn off, phase loss, or heatsink over temperature condition.
10	Delay Angle Control	0 to 5 V analog input to control delay angle. 0V → Max Delay Angle; 5V→ Min Delay Angle
11	GND	Return for BAP3012 control circuitry including delay angle control, therefore it must be tied to the return of the customer provided delay angle control voltage
12	Soft Start/Stop	An open contact between pin 11 and pin 12 will cause the output to ramp up to the programmed output voltage in ≈400 mS for maximum output). A closed contact between pin 11 and pin 12 will cause the output to ramp down to 0 volts in ≈100 mS for minimum output voltage.
13	N/C	No Connection
14	GND	GND signal suggested Return for current feedback
15	Current Feedback	This pin presents an output voltage proportional to the output Bridge current for customer use. Contact factory for suggested current transducer and scale factor requirements.

Phase Reference Options J9 and J10

The default method of deriving phase references is to sense the cathodes of the SCRs on J2 and J4. This is a convenient point to obtain the utility inputs, which are then attenuated and filtered so they can be phase locked to the delayed gate commands. **The magnitude of the utility input must be known when the board is ordered so that the correct components are inserted into the interface circuitry on the board.**

Phase references may also be obtained by using auxiliary connectors J9 and J10 that may be used if the circuit topology does not allow the input voltages to be sensed via the SCR cathodes normally available on J2 and J4. Please refer to Figure 3.

J9 Connector – Phase Reference Input (option) refer to Figure 3

Pin	Signal Name	Description
1	Phase A Reference	Reference input from A2+ SCR
2	Phase B Reference	Reference input from B2+ SCR
3	Phase C Reference	Reference input from C2+ SCR

J10 Connector – Phase Reference Input (option) refer to Figure 3

Pin	Signal Name	Description
1	Phase A Reference	Reference input from A1+ SCR
2	Phase B Reference	Reference input from B1+ SCR
3	Phase C Reference	Reference input from C1+ SCR

Current Limit Control J11

The value of current at which the power supply will fold back can be adjusted with a remote pot connected to J11 or an on-board pot installed in the J11 location. A pot with a resistance of 5KΩ should be used in this application.

Rotating the pot installed in J11 to the fully CW position will result in maximum output current, determined by the scale factor of the Hall Effect Sensor or shunt. Rotating the pot CCW will reduce the amount of current output from the converter bridge. If the impedance of the load decreases while the board is in current limit mode, the delay angle will be increased to reduce the voltage on the bridge in order to keep the current constant.

The BAP3012 can function as a current source controller. By shorting J6-10 to J6-6, the delay angle control voltage will be requesting maximum voltage. The current limit pot, J11, will then control the output current by limiting the delay angle.

J11 Connector – Current Limit Control

Pin	Signal Name	Description
1	High Side	Connected to the high side of the pot
2	Pot Wiper	Connected to the wiper of an external 10K pot
3	Low Side	Connected to the low side of the pot. **This pin is not connected to GND.

Current Feedback J5 and J7

The BAP3012 provides a connectorized interface to two open loop current transducers for current feedback to be used for forcing the currents out of two paralleled bridges to be matched. The total current out of the two bridges is also scaled and fed back to the customer on J6-15. The 4 pin headers on the board interface directly with the HAS, HAC, and HAX open loop Hall Effect sensors from LEM, providing an inexpensive means for obtaining accurate current feedback.

The LEM current transducer, or equivalent, can be placed on either side of the load. Whether it is monitoring the current out of the cathodes (see Figure 2) or the current returning to the anodes, the transducer should be mounted so that the current is flowing in the direction **that provides a positive output.**

If the customer prefers using a shunt to monitor the current, then an interface board may be obtained from APS to perform the necessary isolation and feedback scaling for shunt interface.

J5 and J7 Connector – Current Feedback Inputs

Pin	Signal Name	Description
1	15 VDC	15 VDC
2	-15 VDC	-15 VDC
3	Current Feedback	Voltage proportional to output current
4	GND	GND

Temperature Sense J12

A temperature sensor can be used to interface with the board via J12. The temperature sensor can be mounted on a heatsink to prevent the SCRs from operating at a temperature beyond their ratings. A threshold can be set on the board, so that when the temperature is exceeded, the BAP3012 will inhibit SCR gating and illuminate the OVERTEMP LED.

If heatsink temperature sensing is requested, the APS BAP2161A should be used, mounted near the hottest point of the heatsink assembly. Selecting this option includes a BAP2161A board assembly with mounting instructions.

J12 Connector – Temperature Sense Input

Pin	Signal Name	Description
1	15 VDC	15 VDC
2	Temp	Analog voltage proportional to temperature; 10 mV/°C
3	GND	GND

APPLICATIONS

The following diagrams will provide the user with detailed information for connection and control of several circuit topologies including; paralleled and seriesed converter bridges as well two double star converters, connected in parallel. An explanation of SCR gate connection, current feedback connection, and system interface is included.

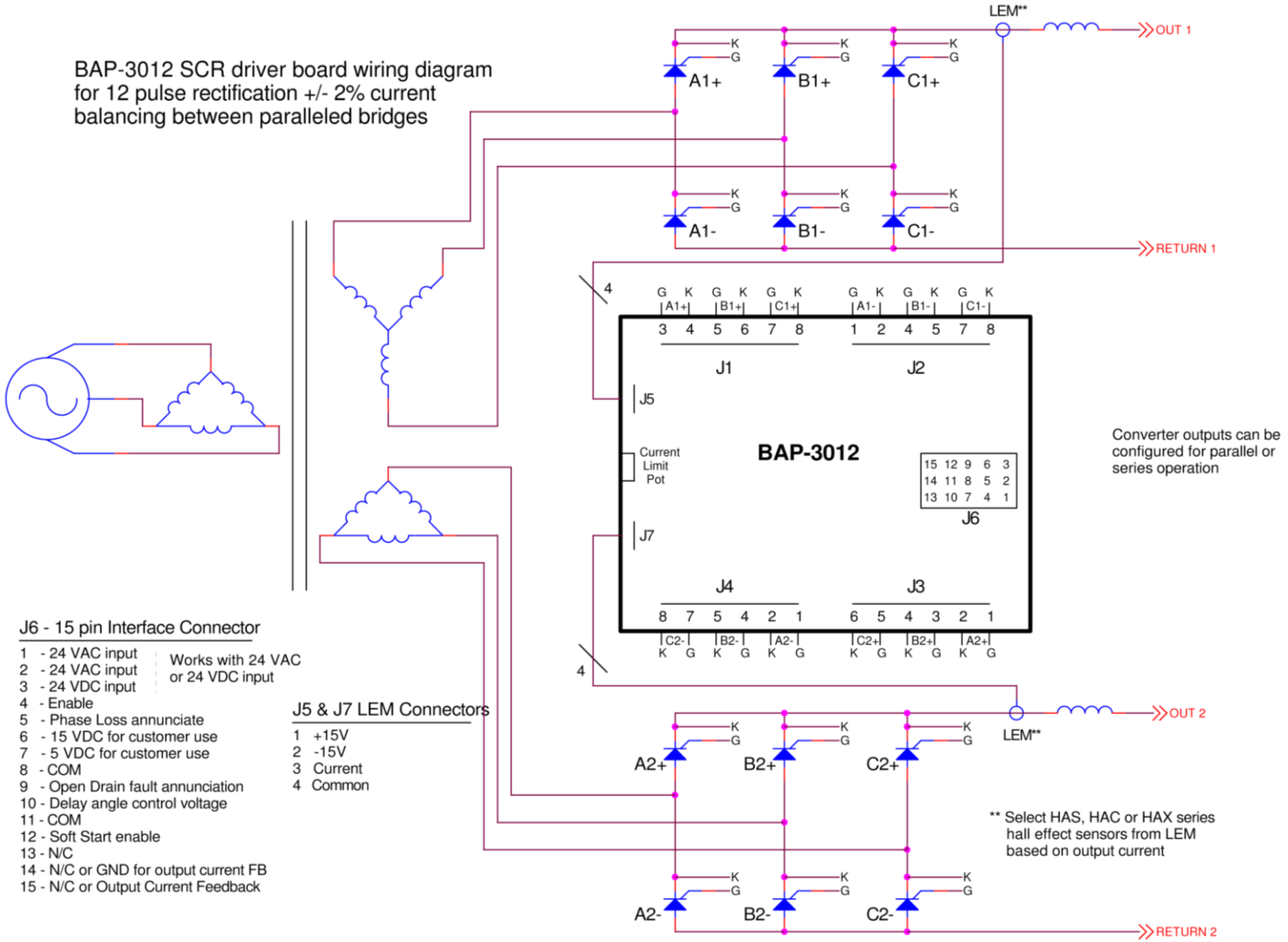

Figure 2: Standard twelve pulse circuit for either series or parallel connection

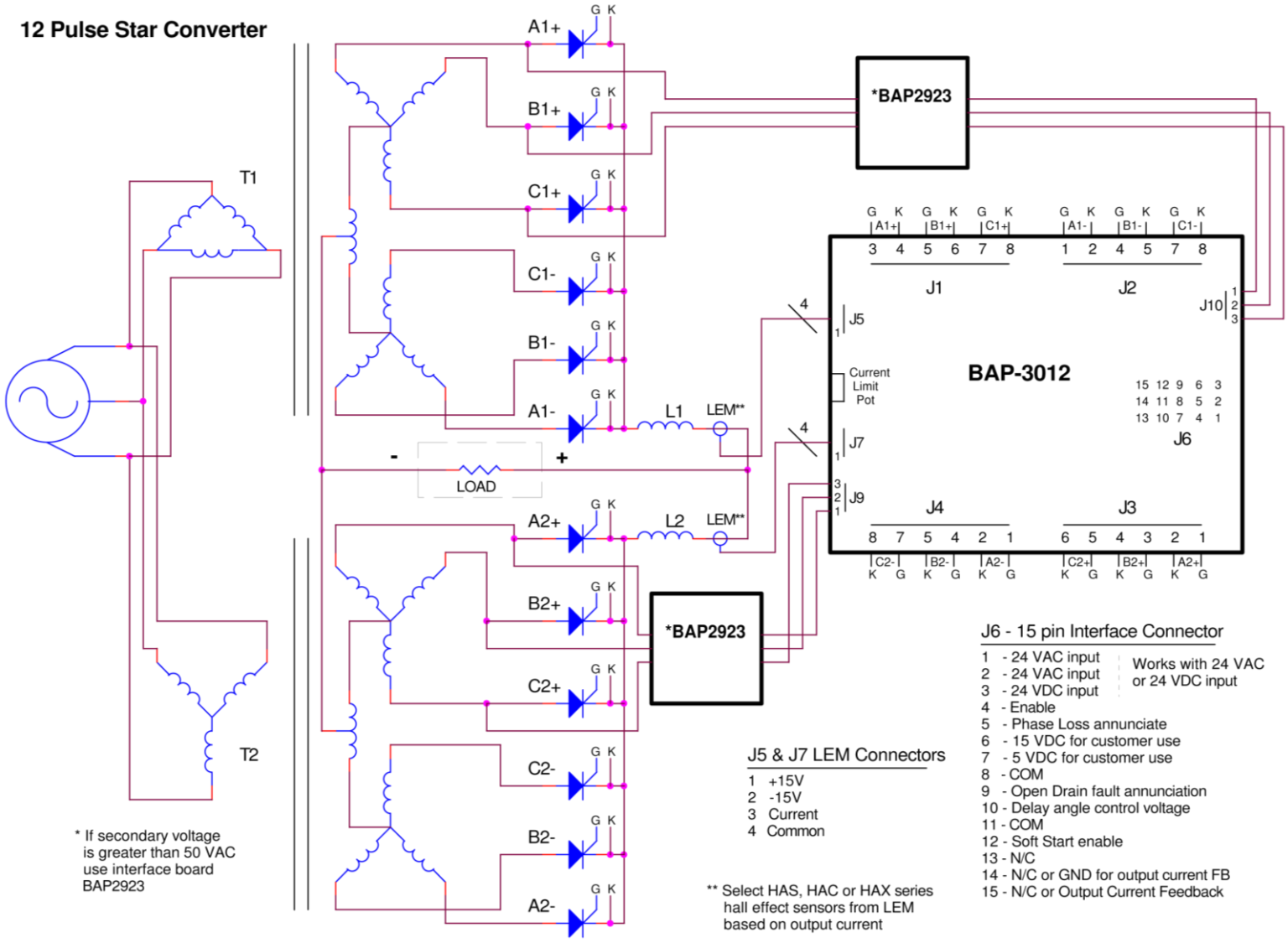

Figure 3: Common Cathode Star Circuit

Absolute Maximum Ratings

Power Supply Voltage AC.....28VAC
Power Supply Voltage DC.....30VDC
Three Phase Voltage 600VAC
Pulse XFMR Isolation.....5,000VAC
Fault Annunciation Pullup
Voltage for J6-9 .....24VDC
Available power sources for Customer use:
24VDC J6-3 .....25mA
15VDC J6-6 .....10mA
5VDC J6-7 .....10mA
Output Curr FB J6-15 .....10mA
Operating Temp .....0-70°C
Storage Temp.....-55°C to +150°C

Electrical Characteristics

Delay Angle Cntrl Voltage* .....0 – 5V
Soft Start Ramp up time* 400mS
Soft Stop Ramp down time*.....100mS
Initial Current pulse peak .....2.4 Amps
Back Porch current 800mA
Open Circuit gate Voltage..... 24volts
Control Board Power Consumption
Idling – pulses inhibited..... 5 VA
Firing pulses..... 15 VA

*adjustable upon customer request

Ordering Information:

BAP3012-X-X-XX-X

Temperature Sense
T – Temperature Sense[1]
0 – No Temperature Sense

Voltage Controlled by SCRs
10 – 10 →100 VAC
11 – 100 → 200 VAC
21 – 200 → 600 VAC

Phase Reference
K – Cathodes sensed on J2 & J4
A – Auxiliary connector J9 & J10

Circuit Topology
P –Converter Bridges - ***Parallel*** Connected
S –Converter Bridges – ***Series*** Connected

[1] Consult factory for OverTemperature threshold settings – heatsink OverTemperature set-point can be set between 40°C and 100°C.