BAP1793 Datasheet and Application Note
Three Phase Fiber Optic Interface Board

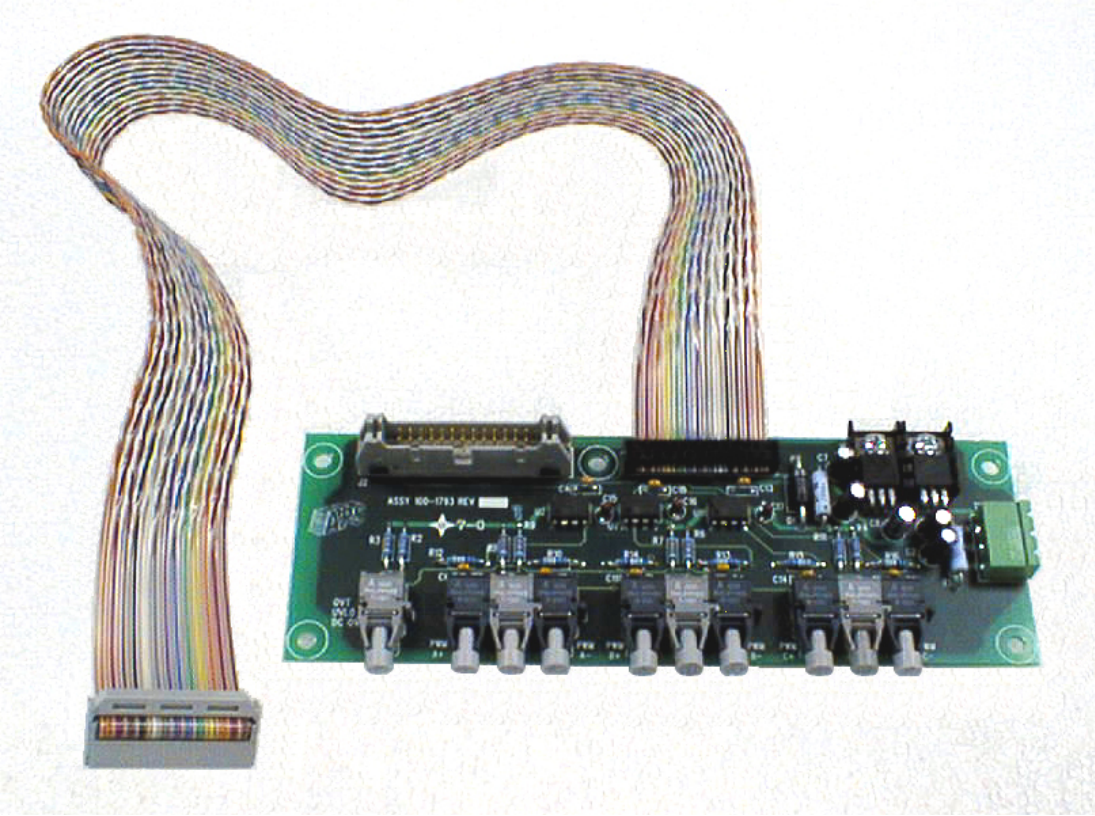

Figure 1: Three Phase Fiber Optic Interface Board

The BAP1793 three-phase fiber optic interface board provides a noise immune interface between a customer provided control board and APS SixPac™ inverter power stage. The PWM control signals from the control board to the fiber optic board (FOB) and the fault signals from the FOB to the control board are transmitted and received via fiber optic cables. This minimizes the effect of electrostatic and electromagnetic interference that is present in proximity to any hard-switched power electronics unit.

The board contains six optical receivers (HFBR-2521), communicating at 5 Mbaud, each of which control the conduction status of the IGBT it controls. Light present at the receiver will turn on the associated IGBT. The IGBT will remain on until the light is removed or until a fault is detected by the SixPac™ gate drive board (GDB), at which point the GDB will latch off and annunciate the fault via the appropriate fiber optic transmitter (HFBR-1521). Light is present at the customer provided control board from the fiber optic transmitter on the FOB when there is no fault to be communicated. This creates a fail-safe condition that latches off the SixPac™ in the event of an unconnected fault signal.

Table 1: Fiber Optic connector functionality

Connector Designation	Part #	Condition with light present	Condition with no light present
PWM A+	HFBR-2521	Upper IGBT of phase A turns ON	Upper IGBT of phase A turns OFF
Ph A OC	HFBR-1521	No Fault	Overcurrent detected on phase A
PWM A-	HFBR-2521	Lower IGBT of phase A turns ON	Lower IGBT of phase A turns OFF
PWM B+	HFBR-2521	Upper IGBT of phase B turns ON	Upper IGBT of phase B turns OFF
Ph B OC	HFBR-1521	No Fault	Overcurrent detected on phase B
PWM B-	HFBR-2521	Lower IGBT of phase B turns ON	Lower IGBT of phase B turns OFF
PWM C+	HFBR-2521	Upper IGBT of phase C turns ON	Upper IGBT of phase C turns OFF
Ph C OC	HFBR-1521	No Fault	Overcurrent detected on phase C
PWM C-	HFBR-2521	Lower IGBT of phase C turns ON	Lower IGBT of phase C turns OFF
OVT, UVLO, DC OV	HFBR-1521	No Fault	Overtemp, Under Voltage Lockout, or DC Overvoltage detected

Table 2: J2 - Signal Descriptions

Pin #	Signal Name	Description
1	Shield	Connected to circuit ground
2	Not Connected	
3	Not Connected	
4	Not Connected	
5	Not Connected	
6	Not Connected	
7	Not Connected	
8	Not Connected	
9	Not Connected	
10	Not Connected	
11	Not Connected	
12	Not Connected	
13	DC Link Voltage	Scaled down analog representation of DC link voltage; 0V represents 0V on DC link, 9V represents 900V on DC link
14	24 VDC input power	20 – 30 VDC input voltage range, tied to pin 15 on the GDB
15	24 VDC input power	20 – 30 VDC input voltage range, tied to pin 14 on the GDB
16	15 VDC input power	14.4 – 15.6 VDC input voltage range, tied to pin 17 on the GDB
17	15 VDC input power	14.4 – 15.6 VDC input voltage range, tied to pin 16 on the GDB
18	GND	Ground reference for 15 and 24 VDC inputs
19	GND	Ground reference for 15 and 24 VDC inputs
20	Heatsink Temperature	Analog voltage representation of heatsink temperature; 0V represents 0°C, 10V represents 120°C
21	GND[1]	Tied to pins 18 and 19
22	I_{out} Phase A	Analog voltage representation of phase A output current; 0V represents 0A, 8V represents rated I_{peak}, -8V represents $-I_{peak}$
23	GND[1]	Tied to pins 18 and 19
24	I_{out} Phase B	Analog voltage representation of phase B output current; 0V represents 0A, 8V represents rated I_{peak}, -8V represents $-I_{peak}$
25	GND[1]	Tied to pins 18 and 19
26	I_{out} Phase C	Analog voltage representation of phase C output current; 0V represents 0A, 8V represents rated I_{peak}, -8V represents $-I_{peak}$

[1] GND signals to be used for analog feedback signals, i.e. twisted pair with I_{out} Phase A.

Input power is connected to the Fiber Optic Interface board at TB1 (see **Figure 2** below). Use one of the two power connections illustrated below, DO NOT connect a 24V supply and a 15V supply to the fiber optic board at the same time. This power is conducted to the GDB through the ribbon cable attached to J1 (see Table 3).

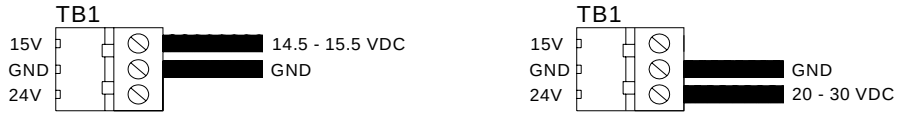

Figure 2: Input power connection diagram

Table 3: J1 – Signal Descriptions

Pin #	Signal Name	Description
1	Shield	Connected to circuit ground
2	PWM A-	0-15 V signal controlling the duty cycle of A- IGBT
3	Phase A Error	Open collector output, external pull-up resistor required LOW = No Error – Light present at PH A OC transmitter on FOB
4	PWM A+	0-15 V signal controlling the duty cycle of A+ IGBT
5	PWM B-	0-15 V signal controlling the duty cycle of B- IGBT
6	Phase B Error	Open collector output, external pull-up resistor required LOW = No Error – Light present at PH B OC transmitter on FOB
7	PWM B+	0-15 V signal controlling the duty cycle of B+ IGBT
8	PWM C-	0-15 V signal controlling the duty cycle of C- IGBT
9	Phase C Error	Open collector output, external pull-up resistor required LOW = No Error– Light present at PH C OC transmitter on FOB
10	PWM C+	0-15 V signal controlling the duty cycle of C+ IGBT
11	Overtemp	Open collector output, external pull-up resistor required LOW = No Error; Floating = heatsink overtemp
12	Not Connected	
13	DC Link Voltage	Scaled down analog representation of DC link voltage; 0V represents 0V on DC link, 9V represents 900V on DC link when using 1200V IGBTs; 9V represents 450V on DC link when using 600V IGBTs.
14	24 VDC input power[1]	20 – 30 VDC input voltage range, tied to pin 15 on the GDB
15	24 VDC input power[1]	20 – 30 VDC input voltage range, tied to pin 14 on the GDB
16	15 VDC input power[1]	14.4 – 15.6 VDC input voltage range, tied to pin 17 on the GDB
17	15 VDC input power[1]	14.4 – 15.6 VDC input voltage range, tied to pin 16 on the GDB
18	GND	Ground reference for 15 and 24 VDC inputs
19	GND	Ground reference for 15 and 24 VDC inputs
20	Heatsink Temperature	Analog voltage representation of heatsink temperature; 0V represents 0°C, 10V represents 120°C
21	GND	Tied to pins 18 and 19
22	I_{out} Phase A	Analog voltage representation of phase A output current
23	GND	Tied to pins 18 and 19
24	I_{out} Phase B	Analog voltage representation of phase B output current
25	GND	Tied to pins 18 and 19
26	I_{out} Phase C	Analog voltage representation of phase C output current

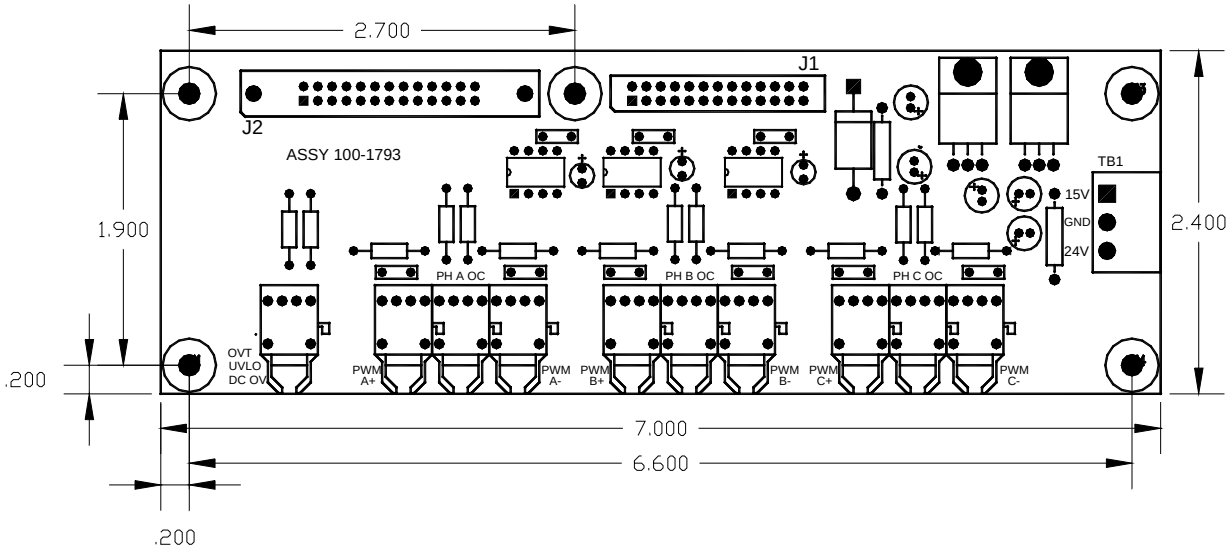

Figure 3: Mechanical dimensions.

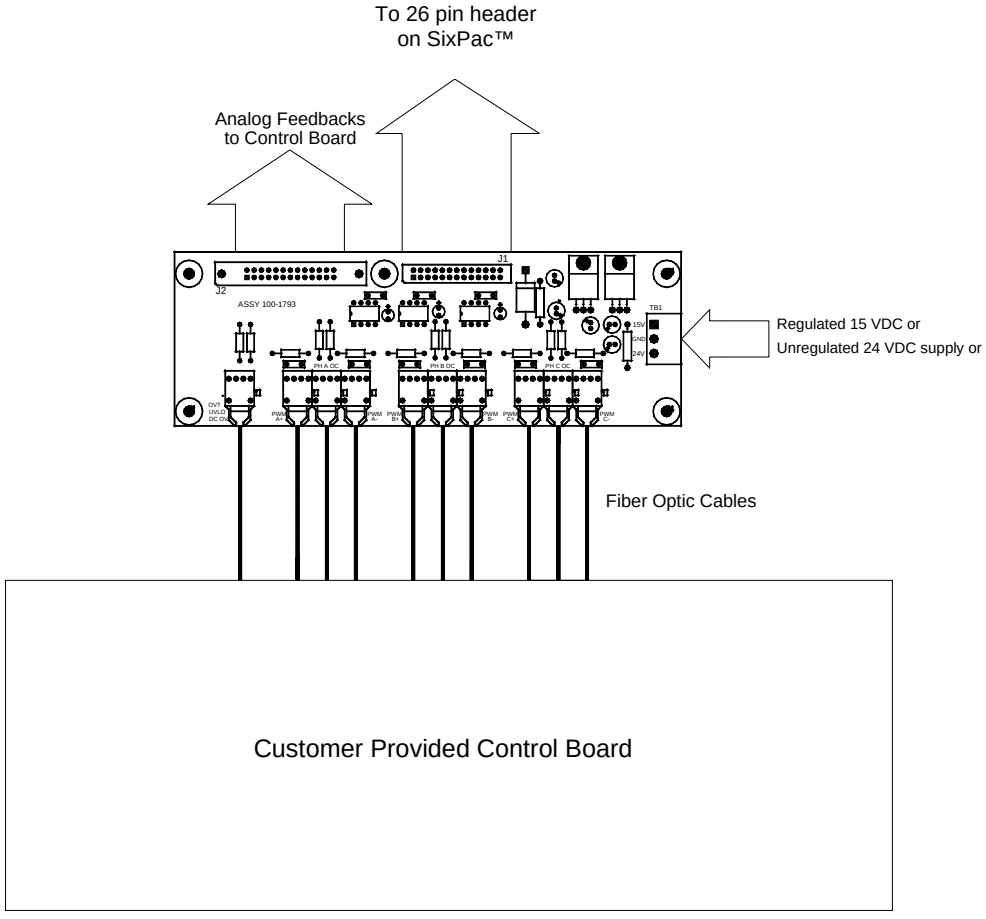

Figure 4: System Connection